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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/736,582 | 12/14/2000 | Harm Peter Hofstee | AUS920000795US1 | 3650 |

7590 07/16/2003

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| EXAMINER |
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2189 | 5 |

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/736,582 | Applicant(s) HOFSTEE ET AL. | |
|---|---|---|---|
| | Examiner Trisha U. Vu | Art Unit 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-19,23-29,31* is/are rejected.

7)☒ Claim(s) *8-10,20-22,30,32-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. Claims 1-36 are presented for examination.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 24-28 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Orr et al. (4,862,350) (herein after Orr).

As to claim 24, Orr teaches a method for executing one or more remote procedure calls comprising the steps of: issuing a plurality of commands by a processing unit (processor 10) to a direct memory access controller (master processor 32) to be executed during one or more remote procedure calls (Fig. 1, col. 1, lines 17-25, and col. 5, lines 27-34), wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit (attached microprocessors) from a memory (shared memory) to said particular attached processing unit (each microprocessor is assigned a specific task) (col. 5, lines 26-34), wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit (col. 11, lines 5-12 and 49-62); issuing to said particular attached processing unit an indication to start a particular operation on said data associated with

said particular attached processing unit instructions (after the master processor polls the attached microprocessors) (col. 11, lines 42-48); and polling a status line of each of a plurality of attached processing units to determine if any of said plurality of attached processing units completed its particular operation; wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls (note the abstract and col. 3, lines 12-20).

As to claim 25, Orr further teaches the attached processing unit instructions enable said particular attached processing unit to perform said particular operation (col. 5, lines 26-34).

As to claim 26, Orr further teaches said indication to start said particular operation on said data is issued from said direct memory access controller to said particular attached processing unit (col. 11, lines 42-48).

As to claim 27, Orr further teaches interrupting said processing unit at a synchronization point (by handshaking), wherein said synchronization point occurs after said one or more remote procedure calls are performed (col. 7, lines 6-29).

As to claim 28, further teaches the direct memory access controller comprises a plurality of first level queues (message buffer) for storing said plurality of commands (col. 9, lines 26-59 and col. 11, lines 49-62).

As to claim 31, Orr further teaches the first and second instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit (col. 11, lines 5-12 and lines 49-62).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-7, 11-14, 16-19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orr et al. (4,862,350) (herein after Orr) in view of Applicant's Admitted Prior Art (herein after AAPA).

As to claim 1, Orr teaches a system comprising a shared memory (shared memory 20); and a processing element coupled to said memory (Fig. 1), wherein said processing element comprises a processing unit (processor 10), a direct memory access controller (master processor 32) and a plurality of attached processing units (microprocessors 22, 24, 26,...), wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls (col. 5, lines 26-34), wherein each of said plurality of attached processing units does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls (note the abstract and col. 3, lines 12-20). However, Orr does not explicitly disclose the system comprises a plurality of processing elements. AAPA teaches a system with a plurality of processing elements (SMP) (page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement multiple processing elements as taught

by AAPA in the system of Orr to improve the processing speed and transaction throughput.

As to claim 13, Orr teaches a system comprising a shared memory (shared memory 20); and a processing element coupled to said memory (Fig. 1), wherein said processing element comprises a processing unit (processor 10), a direct memory access controller (master processor 32) and a plurality of attached processing units (microprocessors 22, 24, 26,...), wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls (col. 5, lines 26-34), wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls (note the abstract and col. 3, lines 12-20). However, Orr does not explicitly disclose the system comprises a plurality of processing elements. AAPA teaches a system with a plurality of processing elements (SMP) (page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement multiple processing elements as taught by AAPA in the system of Orr to improve the processing speed and transaction throughput.

As to claims 2 and 14, Orr as modified above further teaches the direct memory access controller comprises a plurality of first level queues (message buffer) for storing said plurality of commands issued by said corresponding processing unit (col. 9, lines 26-59 and col. 11, lines 49-62).

As to claims 4 and 16, Orr further teaches the plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from said shared memory to said particular attached processing unit (each microprocessor is assigned a specific task) (col. 5, lines 26-34), wherein said plurality of commands comprises a second instruction to copy data associated with said attached processing unit instructions form said shared memory to said particular attached processing unit (col. 11, lines 5-12 and 49-62).

As to claims 5 and 17, Orr further teaches the attached processing unit instructions associated with said particular attached processing unit comprise instructions that enable said particular attached processing unit to perform a particular operation on said data associated with said attached processing unit instructions associated with said particular attached processing unit (col. 5, lines 26-34).

As to claims 6 and 18, Orr further teaches the commands comprise a third instruction to copy the results of said particular operation to said shared memory (col. 5, lines 49-58).

As to claims 7 and 19, Orr further teaches the first and second instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit (col. 11, lines 5-12 and lines 49-62).

As to claim 11, Orr further teaches the direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said on or more remote procedure calls (note the abstract and col. 11,lines 39-48).

As to claims 12 and 23, Orr further teaches the direct memory access controller is configured to interrupt said corresponding processing unit at a synchronization point (by handshaking) wherein said synchronization point occurs after said one or more remote procedure calls are performed (col. 7, lines 6-29).

4. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orr et al. (4,862,350) (herein after Orr) in view of Applicant's Admitted Prior Art (herein after AAPA) as applied to claims 2 and 14 above, and further in view of Goyal et al. (6,055,579) (herein after Goyal).

As to claims 3 and 15, Orr and AAPA do not explicitly teach each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit. Goyal teaches a plurality of command queues wherein each of the command queues is to store the commands associated with different attached processing unit (processing engines) (col. 10, lines 55-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a plurality of command queues wherein each queue is configured to store the commands associated with different processing engine as taught by Goyal in the system of Orr and AAPA so that the processing activities of each of the processing engine are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency (col. 4, lines 15-26).

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Orr et al. (4,862,350) (herein after Orr) as applied to claim 27 above, and further in view of Goyal et al. (6,055,579) (herein after Goyal).

As to claim 29, Orr does not explicitly teach each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit. Goyal teaches a plurality of command queues wherein each of the command queues is to store the commands associated with different attached processing unit (processing engines) (col. 10, lines 55-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a plurality of command queues wherein each queue is configured to store the commands associated with different processing engine as taught by Goyal in the system of Orr so that the processing activities of each of the processing engine are efficiently coordinated for optimal data throughput with minimum idling of processing engines, software processing overhead and latency (col. 4, lines 15-26).

***Allowable Subject Matter***

6. Claims 8-10, 20-22, 30, 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 8, 20, and 30 include the limitation of the direct memory access controller comprises a second queue, wherein the plurality of commands in the plurality of first queues are

merged in said second queue, which is not shown by the prior art of record, in the combination as disclosed and claimed.

Claim 34 includes the limitation of the memory access controller comprises a second queue, wherein the plurality of commands in the plurality of first queues are expanded in said second queue, which is not shown by the prior art of record, in the combination as disclosed and claimed.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art teaches direct memory access in multiprocessing system:

US Patent 6,128,728 Dowling

US Patent 5,634,099 Andrews et al.

and shared processing resource with plurality of processing modules:

US Patent 6,549,881 Dearth et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Trisha U. Vu
Examiner
Art Unit 2189

uv
July 10, 2003

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100